Code :9A04306 **R9**

II B.Tech I Semester(R09) Supplementary Examinations, May 2011
DIGITAL LOGIC DESIGN
(Computer Science & Engineering)

Time: 3 hours **Max Marks: 70**

Answer any FIVE questions
All questions carry equal marks

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1. (a) Convert the following numbers:
   i. $(4D.56)_{16} = ()_2$
   ii. $(231)_4 = ()_{10}$
   (b) Perform the following binary multiplication operations
   i. 100010 X 001010 =
   ii. 000100 X 010101 =
   (c) Explain about error detecting codes with examples?
2. (a) If $\overline{A}B + C\overline{D} = 0$, then prove that $AB + \overline{C}(\overline{A} + \overline{D}) = AB + BD + \overline{BD} + \overline{A}\,\overline{CD}$.
   (b) Realize $Y = A + BC\overline{D}$ using NAND gates.
   (c) Explain about Positive, Negative and mixed logic in binary signals.
3. (a) Using the K-map method. Simply the following function and obtain
   i. Minimal SOP and
   ii. Minimal POS expressions
   $Y = \sum_m (0, 2, 3, 6, 7) + \sum_d (8, 10, 11, 15)$
   (b) Realize the following function as
   i. Multi level NAND-NAND gate network and
   ii. Multi level NOR-NOR network.
   $f = B(A + CD) + A\overline{C}$
4. (a) A combinational logic circuit is defined by the following Boolean functions.
   $F_1 = \overline{A\overline{B}C} + AC, F_2 = A\overline{B}\overline{C} + \overline{A}B, F_3 = \overline{A\overline{B}}C + AB$
   Design the circuit with a decoder and external gates.
   (b) Design a circuit to convert Excess-3 code to BCD code using a 4-bit Full adder.
5. (a) Write the HDL behavioral Description of a
   i. D Flip-Flop
   ii. T Flip Flop
   (b) Draw the circuit diagram of J-K Flip flop with NAND gates with positive edge triggering and explain its operation with the help of truth table. How race around condition is eliminated?
6. (a) Explain Synchronous and ripple counters compare their merits and demerits.
   (b) Draw the block diagram and explain the operation of serial transfer between two shift register and draw its tinning diagram.
7. (a) Explain the block diagram of a memory unit. explain the read and write operation a RAM can perform.
   (b) Derive the PLA programming table and the PLA structure for the combinational circuit that squares a 3-bit number. Minimize the no. of product terms.
8. (a) Describe the design procedure for Asynchronous sequential circuits.
   (b) Obtain a static hazard free asynchronous circuit for the following switching function
   $f(A, B, C) = \overline{Z_m}(1, 3, 6, 7)$

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